IN THE CLAIMS:

None of the claims have been amended herein.

1. (Previously Presented) A semiconductor device having a memory comprising:

a memory array including a plurality of memory cells and a plurality of pairs of complementary digit lines coupled to at least one memory cell of the plurality of memory cells; and

a plurality of sense amplifiers, each sense amplifier of the plurality of sense amplifiers including:

isolating circuitry coupled between an equilibrate bias node of the memory and one pair of digit lines of the plurality of pairs of complementary digit lines of the memory array for isolating the one pair of digit lines from the equilibrate bias node and a cell plate voltage thereon during a margin test mode of the memory, the cell plate voltage including one of a voltage less than a supply voltage and a voltage substantially the same as the supply voltage; and

switching circuitry coupled to the one pair of digit lines for providing a ground voltage during the margin test mode for stressing substantially simultaneously at least one memory cell of the plurality of memory cells of the memory array, the switching circuitry including at least one transistor.

2. (Previously Presented) The semiconductor device of claim 1, wherein the switching circuitry comprises one or more NMOS transistors.

3. (Previously Presented) The semiconductor device of claim 1, wherein the cell plate voltage comprises one-half of the supply voltage of the memory.